WE CLAIM:

1. An MR head biasing circuit comprising:

an MR head;

a constant-voltage and constant-current biasing loop; and

a common-mode feedback loop operatively coupled to the MR head and the constant-voltage and constant-current biasing loop for maintaining the MR head potential at approximately zero Volts.

2. The MR head biasing circuit according to claim 1 wherein the common-mode feedback loop further comprises:

a first current source operatively coupled to a first terminal of the MR head; and

a second current source operatively coupled to a second terminal of the MR head and to the first current source;

whereby the first and second current sources are arranged for minimizing current differential between the first current source and the second current source ~~mirror~~.

3. The MR head biasing circuit according to claim 2 further comprising a central node defined by an operative coupling of the current sources with the first and second terminals of the MR head for maintaining the MR head potential at approximately zero Volts.

4. The MR head biasing circuit according to claim 3 further comprising a reference current source operatively coupled between the central node and a bottom rail.

5. The MR head biasing circuit according to claim 1 wherein the common-mode feedback circuit further comprises:

a first bipolar transistor having an emitter coupled to a top rail of the circuit;

a second bipolar transistor having a base coupled to a base of the first bipolar transistor, the second bipolar transistor also having an emitter coupled to the top rail and a collector coupled to the base;

a third bipolar transistor having a base coupled to a bottom rail via a resistor and a collector coupled to a collector of the first bipolar transistor;

a common-mode feedback current source having a first terminal coupled to an emitter of the third bipolar transistor and having a second terminal coupled to the bottom rail;

a fourth bipolar transistor having an emitter coupled to the first terminal of the common-mode feedback current source and to the emitter of the third bipolar transistor, and also having a collector coupled to the collector of the second bipolar transistor;

a central node defined by the operative coupling of a base of the fourth bipolar transistor, and the first and second terminals of the MR head for maintaining constant voltage.

6. The MR head biasing circuit according to claim 5 wherein the bipolar transistors comprise JFETs.

7. The MR head biasing circuit according to claim 5 wherein the bipolar transistors comprise MOSFETs.

8. The MR head biasing circuit of claim 5 further comprising a stabilizing network coupled between the central node and the first and second MR head terminals.

9. The MR head biasing circuit of claim 8 wherein the stabilizing network further comprises:

a first resistor coupled between the central node and a first terminal of the MR head and a second resistor coupled between the central node and a second terminal of the MR head.

10. The MR head biasing circuit of claim 8 wherein the stabilizing network further comprises:

a first resistor coupled between the central node and a collector of a fifth bipolar transistor;

a second resistor coupled between the central node and a collector of a sixth bipolar transistor;

a third resistor coupled between a location between the first and second resistors and ground; wherein

an emitter of the sixth bipolar transistor is coupled to a bottom rail;

a base of the sixth bipolar transistor is operatively coupled to the constant-voltage biasing loop and also to the MR head;

an emitter of the fifth bipolar transistor coupled to the top rail; and

a base of the fifth bipolar transistor operatively coupled to the collector of the first bipolar transistor and also to the MR head.

11. The MR head biasing circuit according to claim 10 wherein the bipolar transistors comprise JFETs.

12. The MR head biasing circuit according to claim 10 wherein the bipolar transistors comprise MOSFETs.

13. An MR head biasing circuit comprising:

an MR head;

a constant-voltage and constant-current biasing loop; and

a common-mode feedback loop operatively coupled to the MR head and the constant-voltage and constant-current biasing loop for maintaining the MR head potential at approximately zero Volts, the common-mode feedback loop further comprising:

a first bipolar transistor having an emitter coupled to a top rail of the circuit;

a second bipolar transistor having a base coupled to a base of the first bipolar transistor, the second bipolar transistor also having an emitter coupled to the top rail and a collector coupled to the base;

a third bipolar transistor having a base coupled to a bottom rail via a resistor and a collector coupled to a collector of the first bipolar transistor;

a common-mode feedback current source having a first terminal coupled to an emitter of the third bipolar transistor and having a second terminal coupled to the bottom rail;

a fourth bipolar transistor having an emitter coupled to the first terminal of the common-mode feedback current source and to the emitter of the third bipolar transistor, and also having a collector coupled to the collector of the second bipolar transistor;

a central node defined by the operative coupling of a base of the fourth bipolar transistor, and the first and second terminals of the MR head for maintaining constant voltage;

a first resistor coupled between the central node and a collector of

a fifth bipolar transistor;

a second resistor coupled between the central node and a collector of a sixth bipolar transistor;

a third resistor coupled between a location between the first and second resistors and ground; wherein

an emitter of the sixth bipolar transistor is coupled to the bottom rail;

a base of the sixth bipolar transistor is operatively coupled to the constant-voltage biasing loop and also to the MR head;

an emitter of the fifth bipolar transistor coupled to the top rail; and

a base of the fifth bipolar transistor operatively coupled to the collector of the first bipolar transistor and also to the MR head.

14. The MR head biasing circuit according to claim 13 wherein the bipolar transistors comprise JFETs.

15. The MR head biasing circuit according to claim 13 wherein the bipolar transistors comprise MOSFETs.

16. An MR head biasing method comprising the steps of:

providing constant-voltage biasing to an MR head subcircuit;

mirroring the current in a common-mode feedback subcircuit and substantially eliminating any current differential;

thereby maintaining the potential difference at the MR head to approximately zero Volts.

17. An MR head biasing method according to claim 16 further comprising the step of providing reference current in the common-mode feedback subcircuit.